BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

As rescanning documents *will not* correct images, please do not report the images to the Image Problem Mailbox.

Express Mail Label No.: EL443496530US

NITROGEN IMPLANTATION USING A SHADOW EFFECT TO CONTROL GATE OXIDE THICKNESS IN DRAM SEMICONDUCTORS

BACKGROUND OF THE INVENTION

1. Field of the Invention

The invention relates to fabrication of integrated circuit devices incorporating different thicknesses of gate oxides by using nitrogen implantation. Either angled nitrogen implantation or nitride spacers are used to create a "shadow effect", which limits the nitrogen dose close to the edges of the active area. This reduction of nitrogen does leads to an increased gate oxide thickness at the active area adjacent to the shallow trench and increases the threshold of the parasitic corner device and reduces sub Vt(threshold voltage) and junction leakage.

2. Description of The Related Art

In the arrangement of DRAM cell processing using a shallow trench isolation region to realize a small-size capacitor, gate oxide reliability of support oxides is limited by the thickness of the gate oxide at the AA (active area) corners. Therefore, careful optimization of the AA oxidation, (sacrificial) oxide, and gate oxidation is necessary to create the required AA corner rounding and the oxide thickness at the AA corner. In fact, in all too many instances, the oxide is thinner at the corners than at the AA area.

U.S. Patent 5,330,920 discloses a method of controlling gate oxide thickness in the fabrication of semiconductor devices. The process comprises:

forming a sacrificial gate oxide layer on select locations of a semiconductor substrate surface;

implanting nitrogen ions into the select locations of the substrate through the sacrificial gate oxide layer;

thermally annealing the substrate and sacrificial gate oxide layer to assist pile-up of he nitrogen ions at the semiconductor substrate surface;

removing the sacrificial gate oxide layer; and

thermally forming a gate oxide layer on the silicon semiconductor substrate surface, wherein the select locations having nitrogen ion implanted will have a thinner gate oxide layer than a non-implanted region.

Fabrication of an integrated device using nitrogen implantation is disclosed in U.S. Patent 6,037,639. The process comprises:

providing a channel region defined by a source and drain region of a semiconductor substrate having a gate structure comprising an isolating oxide layer positioned on the channel region and the polysilicon layer positioned on the oxide layer. More specifically, the process comprises forming the nitrogen implanted regions over the semiconductor substrate by implanting nitrogen atoms into those regions and growing spacers from exposed portions of the polysilicon layer. During the spacer growth, the spacer grows vertically as well as laterally extending under the polysilicon edges. Diffusion of nitrogen atoms to the substrate surface forms silicon nitride under the gate edges, which minimizes current leakages into the gate polysilicon.

U.S. Patent 5,920,779 disclose a process for differential gate oxide thickness by nitrogen implantation for mixed mode and embedded VLSI circuits comprising:

providing a semiconductor substrate having a surface, the semiconductor substrate comprising a first region on which a plurality of first MOS devices are to be formed and a second region on which a plurality of second MOS devices are to be formed;

masking the second region and providing a first concentration of a first dopant in the semiconductor substrate at the surface of the first region without doping the second region;

removing the mask over the second region;

masking the first region and providing a second concentration of a second dopant in the semiconductor substrate at the surface of the second region without doping the first region, wherein the second concentration is different than the first concentration;

oxidizing the surface of the semiconductor substrate to grow a first thickness of oxide on the first region of the semiconductor substrate and to grow a second, different thickness of oxide on the second region in a single oxidizing process; and

forming first MOS devices on the first regions of the semiconductor substrate incorporating the first thickness of oxide and forming second MOS devices on the second region incorporating the second thickness of oxide;

wherein the first and second dopants are both nitrogen and the first concentration is greater than the second concentration.

In general, a typical way to achieve two oxide thicknesses in one oxidation step is to make use of local nitrogen implantation to reduce the oxidation rate at the implanted sites.

The use of local nitrogen implementation to achieve two oxidation thicknesses in one oxidation step consist of utilizing the process integration scheme of:

growing of the sacrificial oxide;

implantation of dopants through the sacrificial oxide;

employing a photoresist mask to pattern an integrated circuit that includes the first transistor having a first dielectric thickness and a second transistor having a second dielectric thickness;

implanting nitrogen ions to create dual gate oxide devices;

stripping off the photoresist mask and the sacrificial oxide; and

subjecting the gate to oxidation.

Due to the fact that, in many cases, the gate oxide reliability of support oxide is limited by the thickness of the gate oxide at the AA (active area)

corners, and careful optimization of AA oxidation, sac oxide, and gate oxidation is necessary to create the required AA corner rounding and the oxide thickness at the AA corner, there is a need to limit the dual gate nitrogen dose in the AA to the inner part of the gate area to provide increased gate oxide thickness at the active area corner and thereby increase the threshold of the parasitic corner device, reduce sub Vt(threshold voltage) and junction leakage.

SUMMARY OF THE INVENTION

One object of the present invention is to provide a dual gate oxide process for high performance DRAM systems to limit the dual gate nitrogen dose in the AA adjacent the STI oxide by use of a "shadow effect".

Another object of the present invention is to provide a dual gate oxide process for high performance DRAM systems that limit the dual gate nitrogen dose in the AA to the inner part adjacent the STI oxide by use of a "shadow effect" by eliminating the use of vertical nitrogen ion implantation under non-channeling conditions.

A further object of the present invention is to provide a dual gate oxide process for high performance DRAM systems by utilizing either an angled nitrogen ion implantation or nitride deposition to limit the nitrogen dose in the AA to the inner part adjacent the STI oxide by creating a "shadow effect" from the STI oxide which serves to reduce the N_2 dose at the AA edge to create an increased gate oxide at the AA corner and thereby increase the threshold of the parasitic corner device, and reduce sub Vt (threshold voltage) and junction leakage.

These and other objects of the invention will become more apparent by reference to the Brief Description Of The Drawings and Detailed Description Of The Preferred Embodiment Of The Invention.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a graph comparing thickness reduction factor versus level of nitrogen dosage by implantation for a 800°C dry oxidation in pure oxidation.

FIG. 2 is a diagram depicting nitrogen implantation at a non-vertical angle v with respect to the wafer surface at the normal, in which the AA at the inner part adjacent the STI oxide is under a "shadow effect".

FIG. 3 is a depiction of an alternative integration scheme using a nitride deposition to create the "shadow effect" and in which the shadow is complete without the necessity to use angled nitrogen ion implantation to reduce the dual gate nitrogen dose adjacent the STI oxide.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENT OF THE INVENTION

In general, the invention process scheme for providing angled nitrogen implantation into the gate area to create a "shadow effect" during implantation is accomplished by:

providing an AA(etching, oxidation, fill, planarization, and a pad nitride strip);

growing a sacrificial oxide on the substrate;

providing masking steps for channel implants;

affecting channel implants;

affecting a first angled nitrogen implantation without resist mask to create a "shadow effect" from the STI oxide to reduce the N_2 dose at the AA edge to provide increased thickness gate oxide at the AA corners;

providing a masking step for nitrogen ion implantation; and

affecting a second angled nitrogen implantation to create a "shadow effect" from the STI oxide to reduce the N_2 dose at the AA edge to provide increased thickness gate oxide at the AA corners.

In particular, the process flow for fabricating a dynamic random access memory cell utilizing angled nitrogen implantation of the invention will entail:

1) a. forming the active area by the well-known process of forming over a substrate, a patterned hard mask layer exposing portions of the substrate so as to define an isolation region; ;

b. etching exposed regions of the substrate using the patterned hard mask layer to form an isolation trench in the isolation region;

c. oxidizing the substrate to form a thermal oxide layer in the isolation trench;

d. depositing an oxide layer over the thermal oxide layer to fill unfilled portions of the isolation trench;

e. removing the patterned hard mask;

f. planarizing the substrate and forming a pad nitride strip;

2) forming a sacrificial gate oxide layer in the areas of the semiconductor substrate where the pad nitride has been stripped off;

3) affecting channel implants in selected areas using resist masks;

4) affecting a first low dose angled nitrogen implant without using an implant mask in a manner to limit the nitrogen dose in the active area to the inner part of the gate area so that the angled nitrogen dose in the "shadow part" of the active area is less than the amount of the nitrogen dose implanted in the remaining non-shadowed area (to affect the spatial thickness distribution of all exposed oxide areas);

5) affecting masking so that nitrogen ions (N_2^+) to be implanted do not penetrate the masked region; and

6) affecting a second angled nitrogen ion implantation in a manner so as to limit the dual gate nitrogen dose in the active area to the inner part of the gate area so that the angled nitrogen dose in the "shadow part" of the active area is less than the amount of the nitrogen dose implanted in the remaining non-shadowed area.

In general, nitrogen ion implantation is known to be done vertically under non-channeling conditions in the prior art, where the goal of the nitrogen ion implantation is to create a thinner oxide in the implanted areas, thereby leading to two oxide thicknesses for the non-implanted area and the nitrogen implanted area.

Reference is now made to FIG. 1, which shows a graph of thickness reduction due to N_2 implantation followed by a thermal oxidation in pure oxygen at a temperature of 800° C. The thickness reduction factor is defined as the ratio of the oxide thickness without nitrogen implant divided by the oxide thickness with nitrogen implant.

In the context of the invention process, reference is made to the schematic diagram of FIG. 2 which shows nitrogen ions N_2 implanted under an angle ν with respect to the normal surface of the AA 10 of the wafer surface 11. Two implantations are conducted under $+\nu$ and under $-\nu$. The nitrogen dose in the shadow area of the AA is half the amount of nitrogen ion dose implanted in the remaining, non-shadowed area.

The length of the shadow area x is calculated according to the following formula:

$$\text{Tan } \nu = x/h$$

where h is the height of the STI oxide 12 over the AA surface. When h = 500A (+/- 150A) and ν = 60 degrees the maximum value for x = 866A. If an angle of 15 degrees is chosen, x = 130A (+/- 40A). The shadow length can be chosen over a long range. The goal for x is approximately 10% of the ground rule, e.g. 100A – 170A in the existing microelectronic technologies.

To comprehend the effect of the nitrogen implantation on oxide thickness, thick and thin oxides within the framework of dual gate technology are discussed separately.

1) Thick oxide: In the dual gate process known in the art, the thick oxide is not exposed to a nitrogen implantation. The invention uses a low dose nitrogen implant for the thick oxide to modify and optimize its spatial thickness

distribution. The nitrogen dose is chosen to be 5e13-1e14cm^{-2}. For the case 1e14cm^{-} and using 800°C oxidation, a reduction of the oxide thickness of approximately 20% is achieved in the non-shadow region of the gate. In the shadow regions where only 5e13cm-2 is implanted, the oxide thickness is reduced by only 10%.

2) Thin oxide: The nitrogen dose is chosen to be approximately 4e14cm^{-2}. This gives a reduction of 70% with respect to the non-implanted case, or 50% to the case of the 1e14cm^{-2} implanted thick oxide. The oxide at the STI oxide edges is 35% thicker than in the non-shadow region.

FIG. 3, shows an alternative embodiment of the invention process that provides a "shadow effect" or shadow area SA which is complete or fixed, thereby eliminating the need to utilize angled nitrogen ion implantation and yet, achieve benefits as though angled nitrogen implantation had been used.

In this alternative embodiment of the invention process, the integration scheme utilizes a nitride spacer deposition to provide the shadow effect. In this alternative embodiment, a nitride deposition ND such as that of silicon nitride is performed after the channel implantation steps. Thereafter, optionally, steam oxidation may be employed to convert the nitride layer into an oxide. Following conversion of the nitride layer into an oxide by steam oxidation, vertical implantation of nitrogen ions as shown by the two downwardly pointing arrows is employed. Since the "shadow effect" as shown by x results from the nitride deposition, vertical nitrogen ion implantation still results in less nitrogen ion implantation in the area adjacent the STI oxide 13 as shown by x, than in the active area AA of wafer surface 14.

In this alternative integration scheme of the process of the invention, since the "shadow effect" is complete by virtue of the nitride deposition, it is not necessary to use angled nitrogen ion implantation.